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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,195	09/25/2002	Raj Kumar Jain	2000P19187US	8143

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EXAMINER	
LE, THONG QUOC	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,195	JAIN, RAJ KUMAR	
	Examiner	Art Unit	
	Thong Q. Le	2818	AW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20-22* is/are allowed.

6)☒ Claim(s) *1-7 and 12* is/are rejected.

7)☒ Claim(s) *8-11 and 13-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-7, 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Hsu et al. (U.S. Patent No. 5,923,593).

Regarding claims 1-7, Hsu et al. discloses a memory device (Figure 6), comprising: a memory cell array having a multitude of memory cells (610), first and second bitlines (660, 661), and first and second wordlines (631, 632), each of said memory cells being coupled to one of said first bitlines (Figure 6), one of said second bitlines, one of said first word lines, and one of said second wordlines (Figure 6), each of said memory cells being accessible through one of said first wordlines and one of said first bitlines by an external port and being accessible through one of said second wordlines and one of said second bitlines by an internal (Figure 6) ; said external port being connected to input terminals to receive input signals in order to select one of said memory cells for an external data access', and a refresh control unit generating refresh control signals to access one of said memory cells to perform a refresh of the respective one of said memory cells through said internal port (ABSTRACT, Column 2, lines 12-

50), and wherein each one of said memory comprises : a first selection transistor coupled to one of said first wordlines (Figure 6, 632) and one of said first bitlines (Figure 6, 680A), a second selection transistor coupled to one said second wordlines (Figure 6, 640) and one of said second bitlines (Figure 6, 680B) and a storage node (Figure 4) connected to said first selection transistor and said second selection transistor(Figure 4), and wherein each one of said memory comprises: a storage transistor having a drain/source path and a gate terminal, said drain/source path being connected to said first and said second selection transistors; and said gate terminal being connected to a reference potential (Figure 4) wherein said external port is connected to input terminals designed to receive one of an address signal, signal determining a read or a write operation, a data clock signal, and a device select signal (ABSTRACT), and wherein said internal port is hidden from said address signal, said signal determining a read or a write operation, and said device select signal, and comprising: a first bank of sense amplifiers (Figure 6, 670), wherein each one of said first bitlines is connected to one of said sense amplifiers of said first bank (Figure 6); a column decoder (Figure 5, 520), wherein an individual one of said sense amplifiers of said first bank can be selected to perform one of data read to an external terminal, and data write from an external terminal, and comprising: a second bank of sense amplifiers (Figure 6, 671), wherein each one of said second bitlines is connected to one of said sense amplifiers of said second bank (Figure 6), and wherein multiple of said amplifiers are selected to perform a refresh of a row of memory cells

Regarding claim 12, Hsu et al. disclose a memory device (Figure 6), comprising :

a memory cell array having memory cells (610) , each of said memory cells being accessible through a first port and through a second port, only said first port of said first and second ports being accessible by an external address signal to select one of said memory cells (ABSTRACT); and

a refresh control circuit (Column 2, lines 12-20) designed to generate refresh control signals to refresh said memory cells through said second port (Column 2, lines 41-45).

Allowable Subject Matter

4. Claims 8,-11,13-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 8-11,13-19 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Hsu et al. (U.S. Patent No. 5,923,593), and others, does not teach the claimed invention having a contention detection circuit receiving a refresh address to access a subset of said memory cells and an address to access at least of one said memory cells of said subset of memory cells for an external read or write operation, said contention detection circuit suppressing a refresh operation for said subset of said memory cells.

Claims 20-22 are allowed.

Claims 20-22 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Hsu et al. (U.S. Patent No. 5,923,593), and others, does not teach the claimed invention having a memory device comprises a second row decoder to activate one of said rows in response to an internal address, and a refresh control circuit to refresh the memory cells of a row which is activated by said second row decoder.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2818

THONG LE
PRIMARY EXAMINER